Weekly_MT_20250618

- ASAGI : Summary of Shirotori-san’s lecture @RIKEN etc…
- E80-TC : Observed the raw singals
- E80-CDC : Plan?
- ToDo

“TC” = “Test Chamber”

Yuto Kimura (Tohoku, D1)

ASAGI

- ASAGI lecture by Shirotori-san on June 13, 2025
  - Code for ASAGI was uploaded to the FPGA on HUL board.
  - Parameters (the number of capacitors and resistors on ASAGI) were configured.
  - ASAGI's response to test pulse was observed with using a function generator.
  - ASAGI was connected to the E15-TC, and signals were observed (cosmic and X-ray from 55Fe).
  - More details are provided at back-up part or

    https://drive.google.com/file/d/1FRdHSae8a26mIZH8iAuMz0keBVNoAiUb/view?usp=drive_link.

CSA: Charge Sensitive Amplifier
PZC: Pole Zero Cancelletion
SHA: Shaping amplifier

ASAGI

- Purpose
  - Prepare for the upcoming 16ch version of ASAGI
- What I will do
  - Decide the best parameters by a criteria below;
    - Suppress the tale of the signal (It’s better to set “CSA:PZC” to “2:1”?)
    - Suppress analog signal saturation after SHA
    - Operate at the lowest possible HV and Vth without compromising detection efficiency
  - Understand ASAGI’s response characteristics by changing parameters and input charge with function generator

ASAGI

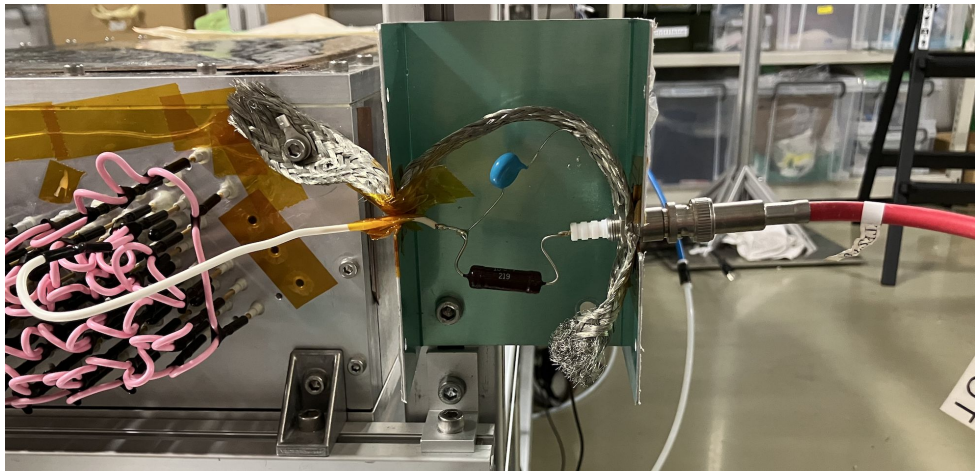
test2pot	10.00 uA	2700.0 V	0.00 uA	2699.5 V	On		30 V/s	70 V/s	0.1
test2gua	10.00 uA	1454.0 V	0.00 uA	1453.8 V	On		20 V/s	70 V/s	0.1
test1pot	10.00 uA	2700.0 V	0.46 uA	2699.0 V	On				0.1
test1gua	10.00 uA	1454.0 V	0.08 uA	1454.3 V	On				0.1

right after turning on

test2pot	10.00 uA	2700.0 V	0.00 uA	2699.5 V	On		30 V/s	70 V/s	0.1
test2gua	10.00 uA	1454.0 V	0.00 uA	1453.8 V	On		20 V/s	70 V/s	0.1
test1pot	10.00 uA	2700.0 V	0.64 uA	2699.0 V	On				0.1
test1gua	10.00 uA	1454.0 V	0.12 uA	1454.3 V	On				0.1

7 minutes later

- Status of E15-TC
  - The current on potential and guard wires is higher than usual for some reason.
    - remade Low-Pass-Filter (GND became stronger) → but not solved…
  - No progress on ASAGI x E15-TC



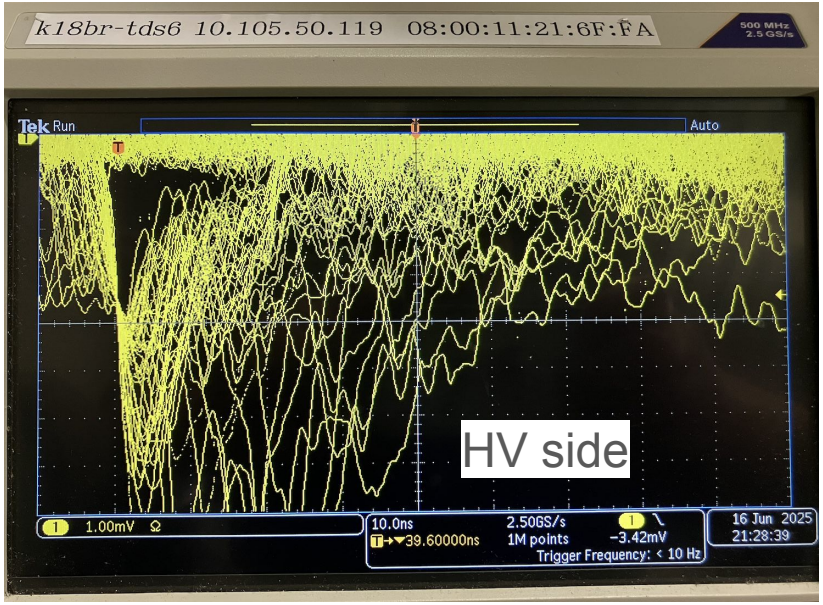
ASAGI

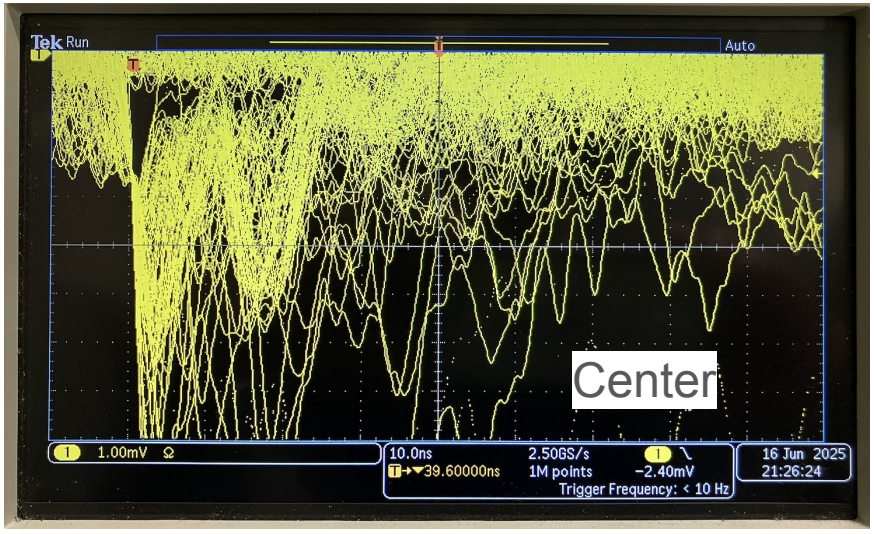
- ASAGI’s response to test pulse
  - plan → do from this week

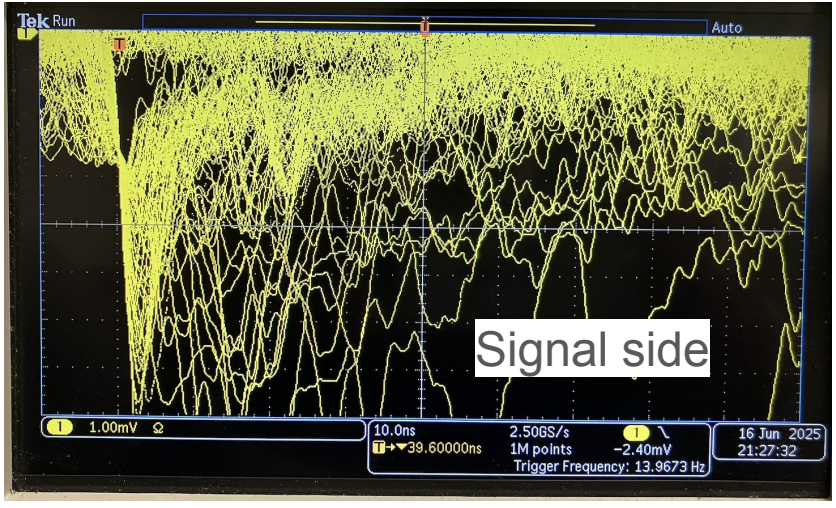
帯域を下げて見てみよ。

E80-TC

2025.06.17時点







⚪reflected wave
? pulse height
→ Can we explain them by taking attenuation into account?

E80-TC

HV of potential tripped because low pass circuit has an issue…

There was no problem until yesterday…

E80-CDC

- Plan
  - July 1~3
    - start to flow Ar-C2H6 and prepare HV moduals
    - construct the HV monitoring system
  - July 11~
    - HV conditioning
  - ???
    - Once we gain confidence in E80-TC, let’s observe the raw signals and pre-amp output in E80-CDC as well.

ToDo

- HYP2025 abstract : E80-CDS, ~ June 30
  - share the first ver. to the local members by this weekend
- JPS application : J-PARC E80 progress status (検出器セッション), ~ July 3
  - share the first ver. to the local members by this weekend
- Summary of the gas study
  - share the first ver. to the local members by this weekend
- (RIKEN Discovery Evening : Poster, July 4
  -)

Back up

ASAGI lecture with Shirotori-san

(June 12-13, 2025)

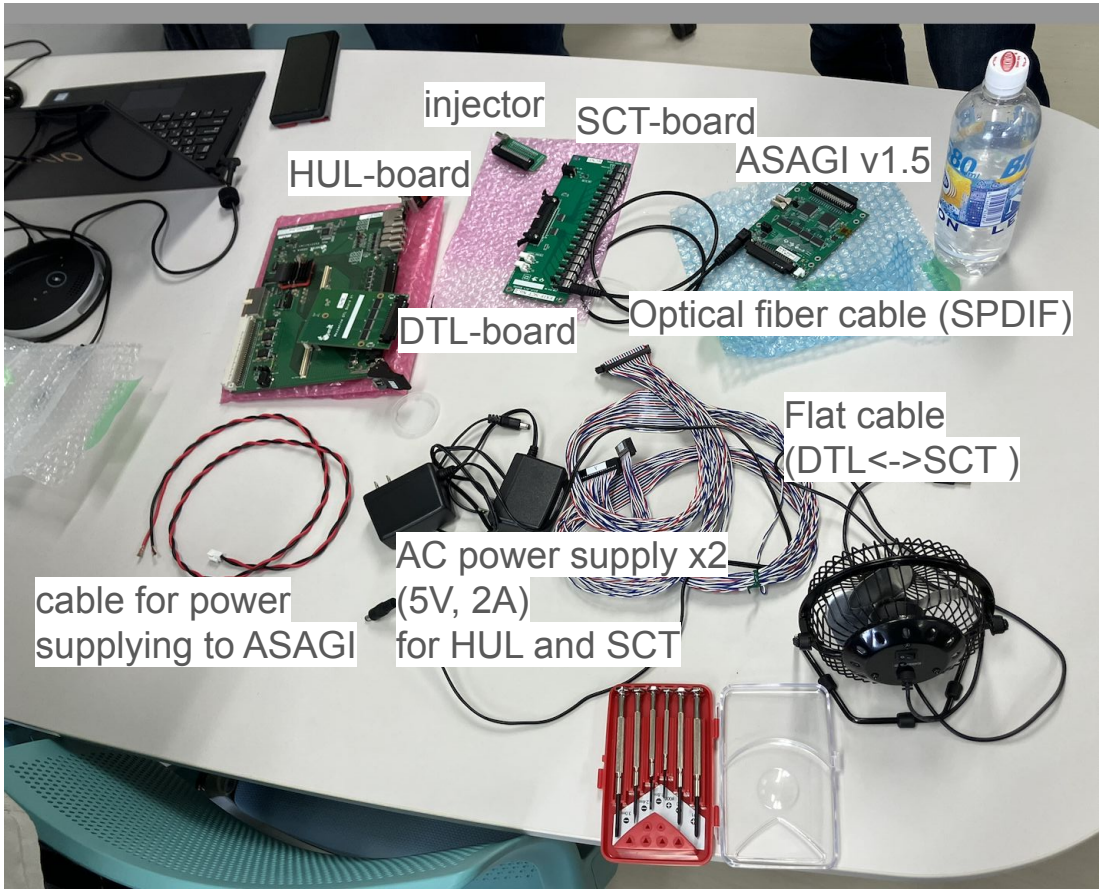
Participants

- K. Shirotori (RCNP, SPADI-A)
- S. Hanai, R. Tsutiya (for SR-PPAC / CNS, HIMAC)
- T. Isobe (for many purposes, RIKEN, RIBF)
- F. Sakuma, T. Hashimoto, Y. Kimura (for CDC / RIKEN, J-PARC)

@ RIBF room 308, RIEKN

1: Configuration of FPGA on HUL

ASAGI v1.5 is to be controlled by an FPGA.
The FPGA on the HUL board can be used.
We first need to program the FPGA for ASAGI, using tools such as Vivado(Xilinx).



2: Setting the parameters

https://drive.google.com/drive/u/1/folders/1wUCWsQm0V-vIDd7yD64iHglbir8E1B7U

ASICのレジスタ設定について

13

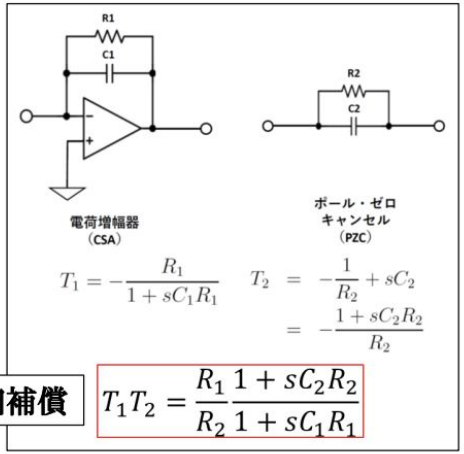
＊32 chの各チャンネルごとに設定可能
- アナログ出力: ある1 chのみを選択
- テスト信号: 各chに分配可能

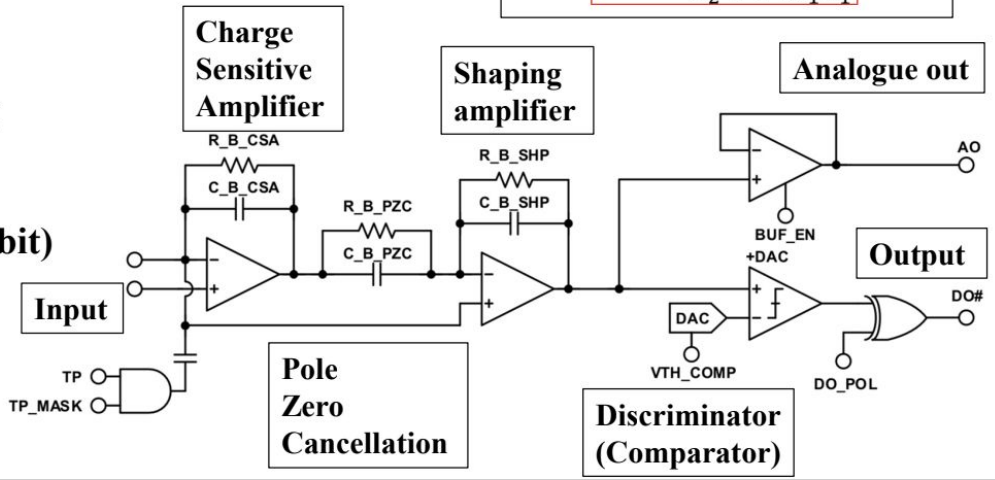
- 電荷増幅器(CSA)とpole-zero回路(PZC)
  - 抵抗(250 kΩ): 1–4個 & 容量(250 fF): 1–8個の接続数
    - 接続数の積は同じ(位相補償): CSA: R×C = PZC: R×C

- 波形整形器(SHP)
  - 抵抗(15 kΩ): 1–4個
  & 容量(250 fF): 1–8個の接続数

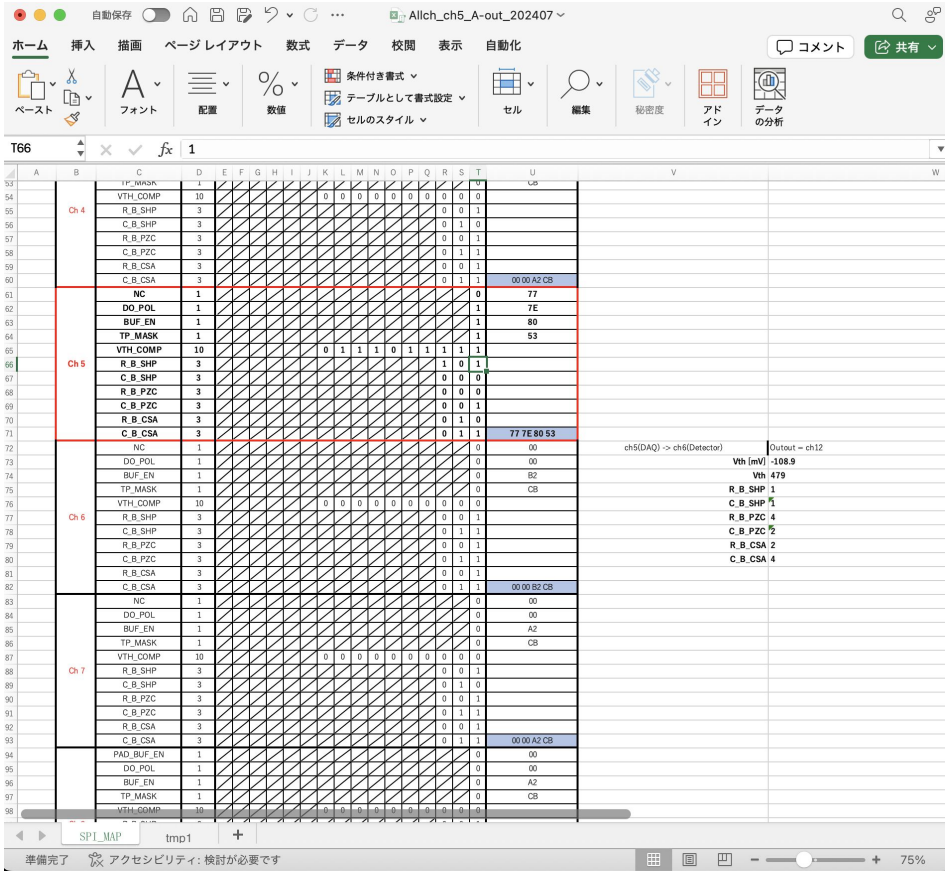
- 閾値(Vth)
  - ±1.65 Vを10 bit刻み(3.3 mV/bit)
    - 0–3.3 Vに1.65 Vのオフセット

- 出力極性
  - 正負を選択可能





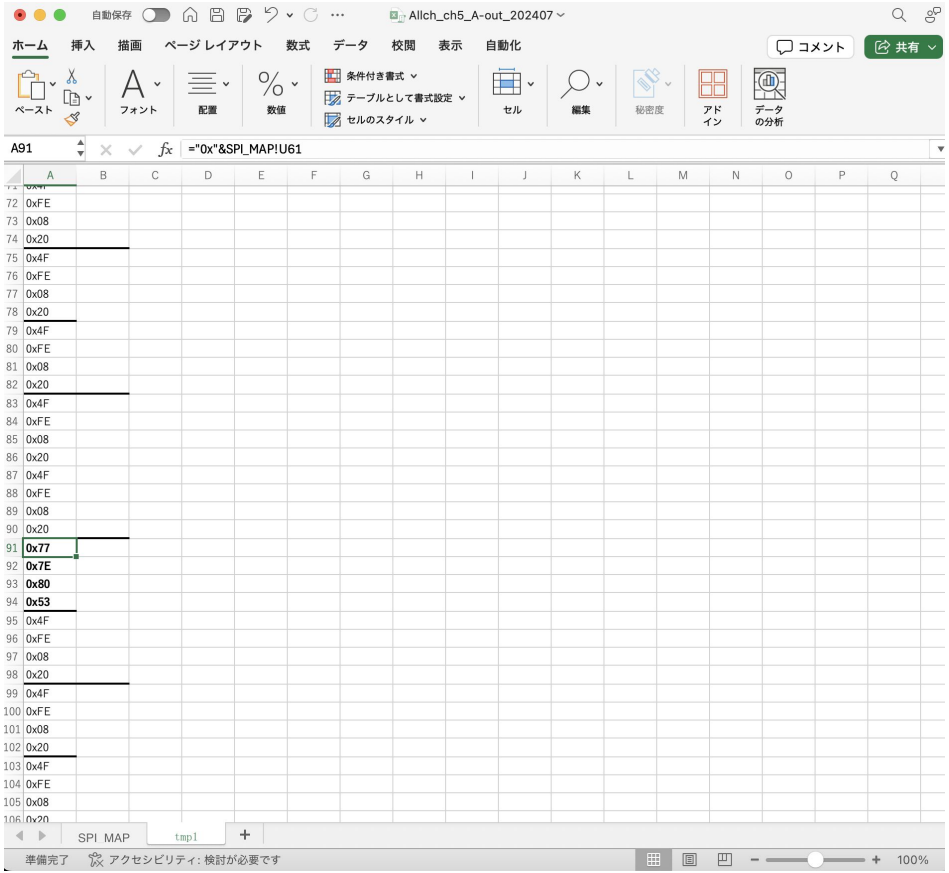
2: Setting the parameters



Rewrite the values inside the red line.

* In this case, now we can see the analog signal of ch12 only.
  But it depends on the settings of the macro program.

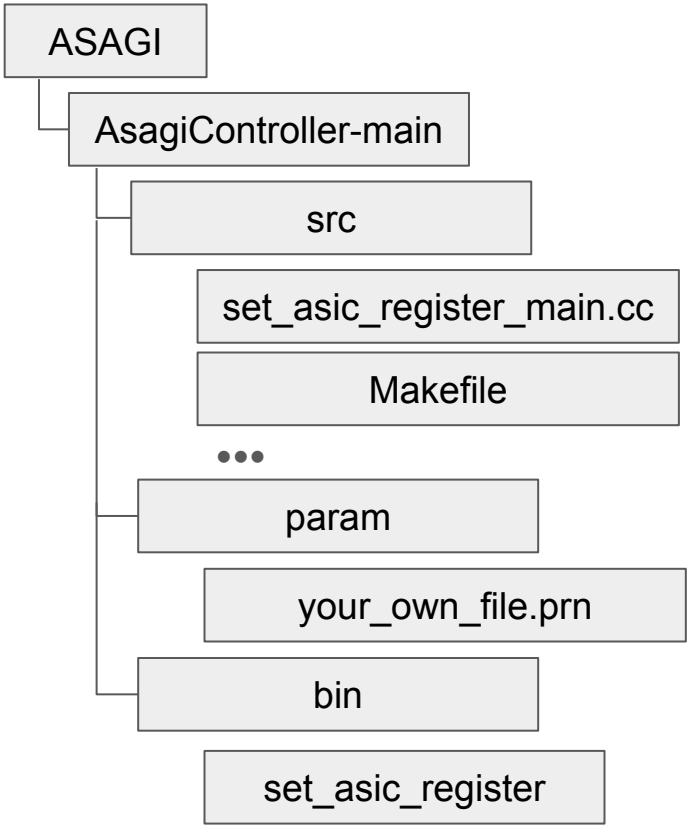
2: Setting the parameters



	A
72	0xFE
73	0x08
74	0x20
75	0x4F
76	0xFE
77	0x08
78	0x20
79	0x4F
80	0xFE
81	0x08
82	0x20
83	0x4F
84	0xFE
85	0x08
86	0x20
87	0x4F
88	0xFE
89	0x08
90	0x20
91	**0x77**
92	**0x7E**
93	**0x80**
94	**0x53**
95	0x4F
96	0xFE
97	0x08
98	0x20
99	0x4F
100	0xFE
101	0x08
102	0x20
103	0x4F
104	0xFE
105	0x08
106	0x20

Save this sheet as a “.prc” file.

3: Make and execute



1 . Make here.

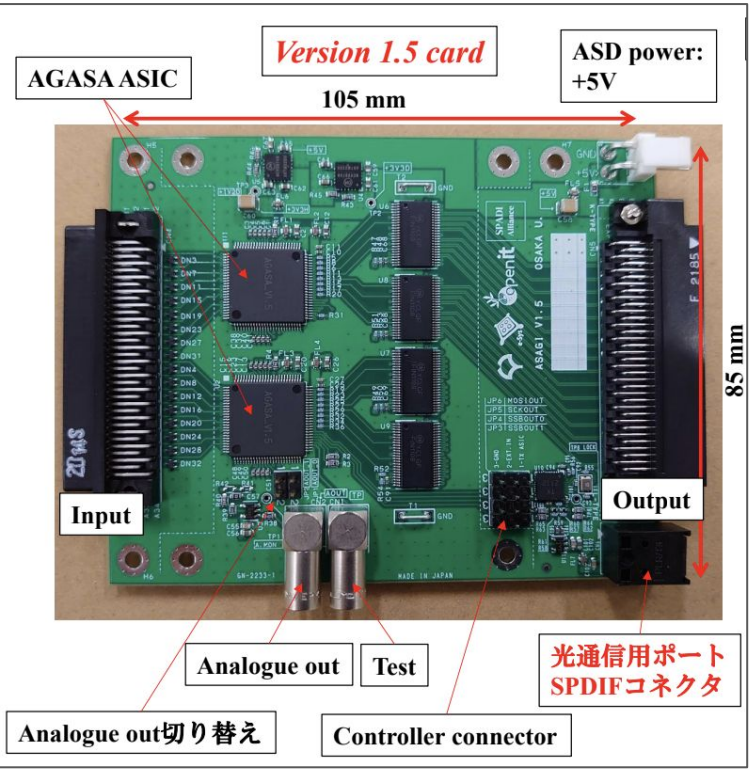
2 . Set your parameters in the Excel file, save it as a .prn file, and put it here.

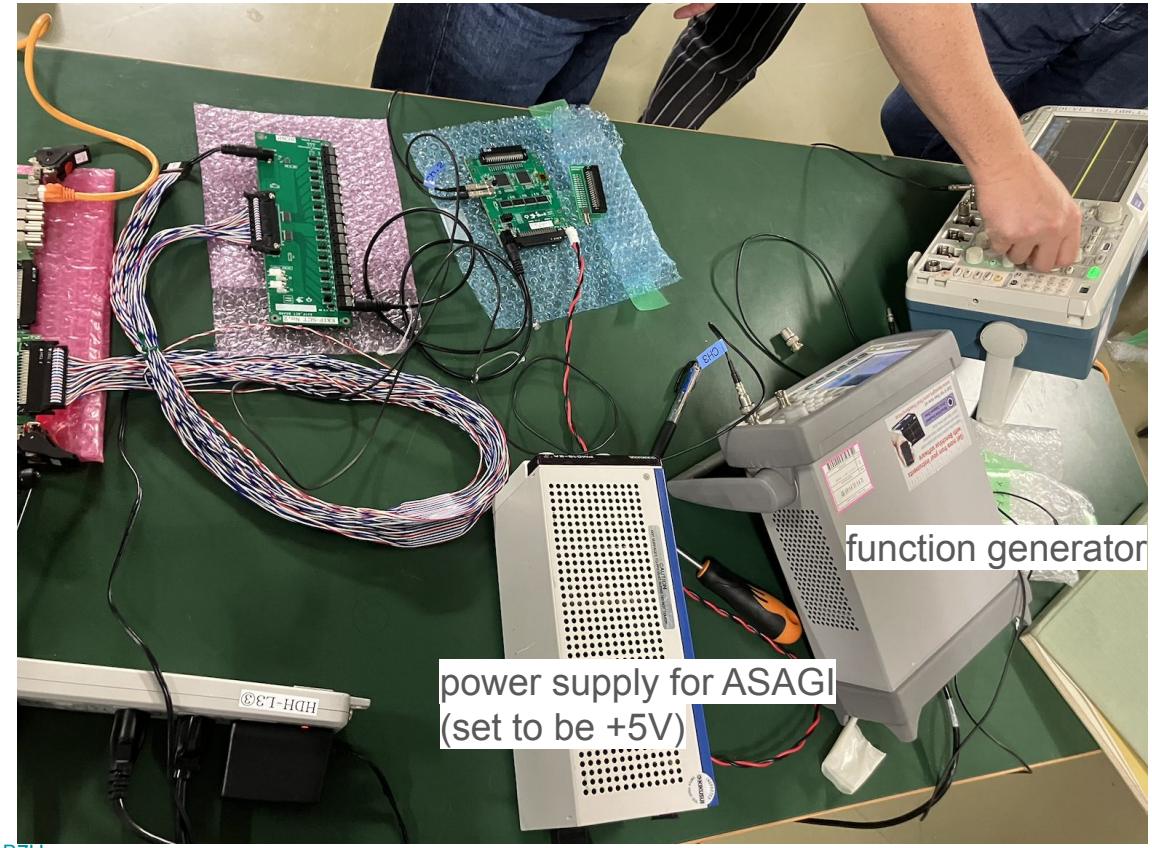
3 . Execute it with a parameter file,
like “./bin/set_asic_register 192.168.1.113 param/test2.prn”.

HUL ip adress

4: Test pulse from a function generator

＊Set to AC mode in oscillo when seeing the analog output, because …

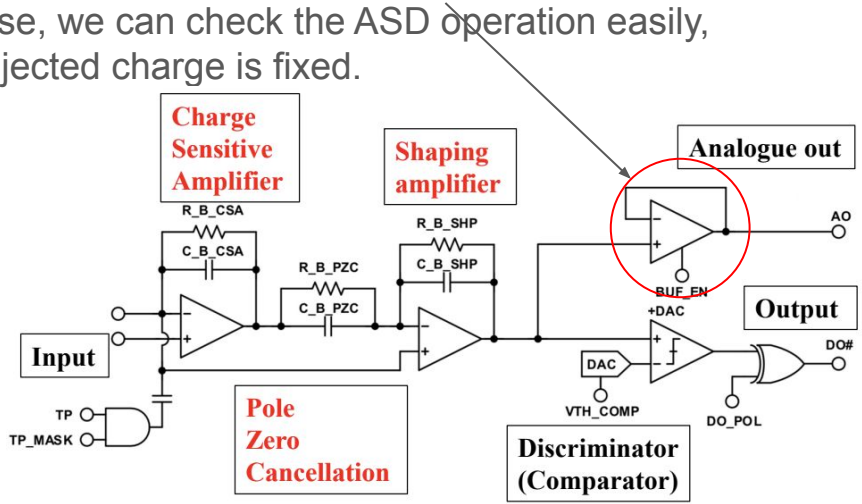


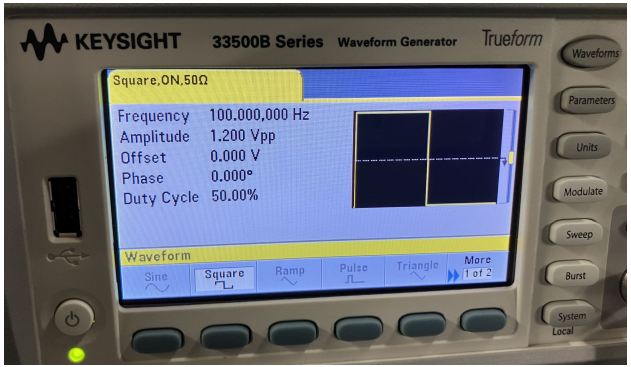


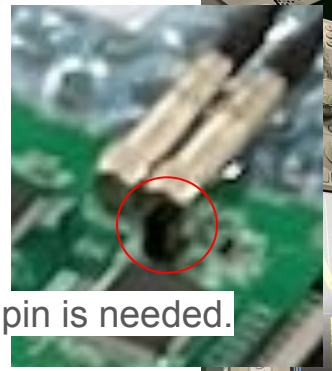
https://drive.google.com/drive/u/1/folders/1wUCWsQm0V-vlDd7yD64iHglbir8E1B7U

4: Test pulse from a function generator (w/o injector)

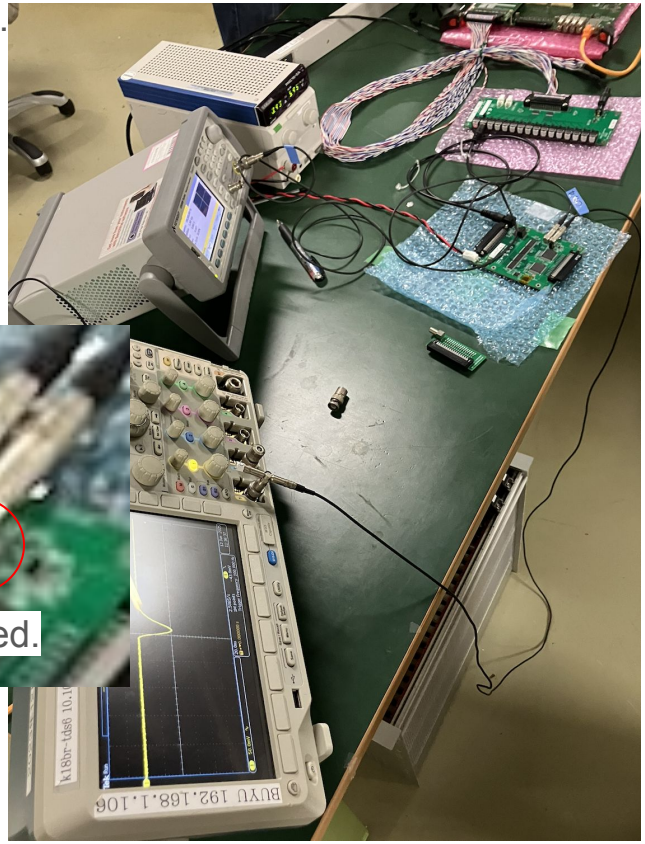
If you want to see the signals after this without injector, set like the pictures.
In this case, we can check the ASD operation easily,
but the injected charge is fixed.







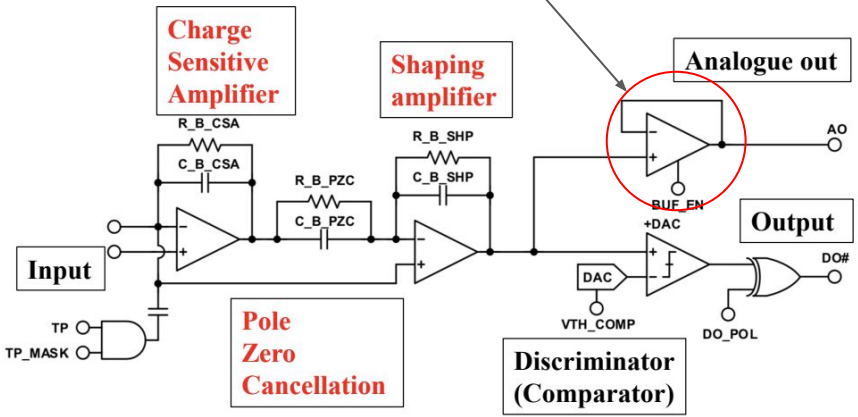
Jumper pin is needed.

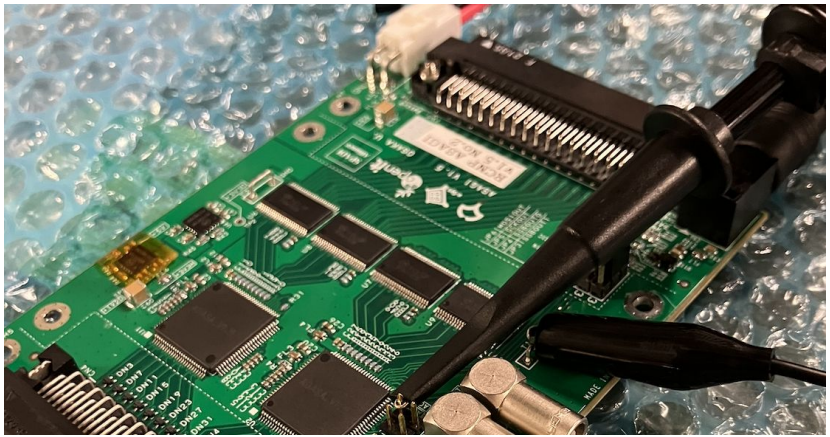


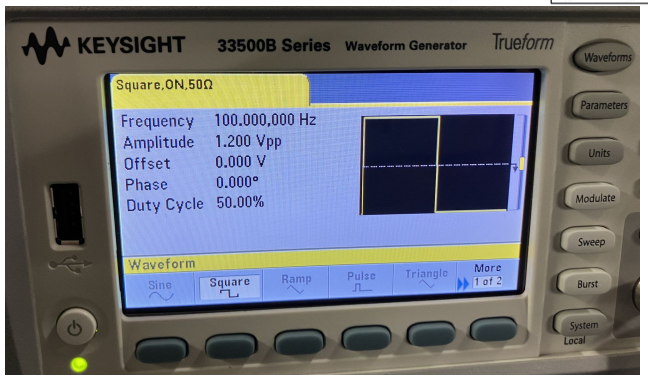
Amplitude should be setted to 1.2V.

4: Test pulse from a function generator (w/o injector)

If you want to see the signals before this without injector, set like the pictures.
In this case, the injected charge is fixed too.
And we need to use a probe to see the signals.







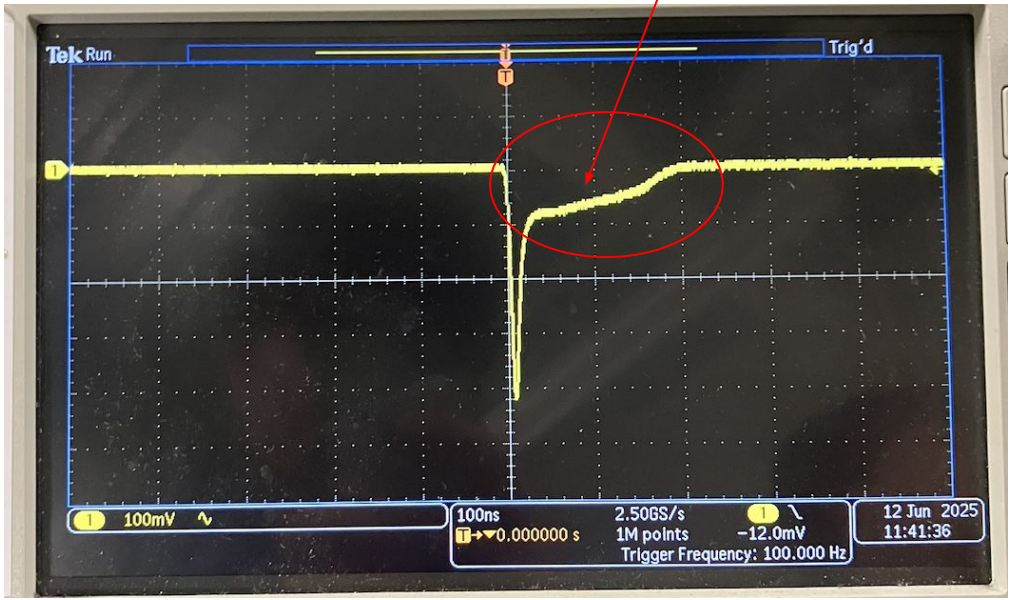
Amplitude should be setted to 1.2V.

5: Test pulse from a function generator (w/ injector)

With the injector, we can control the input signal charge as desired, by just changing the square wave amplitude. (1 pC < Q_in < 3 pC, C = 1 pF (const))

sarturation

for example,

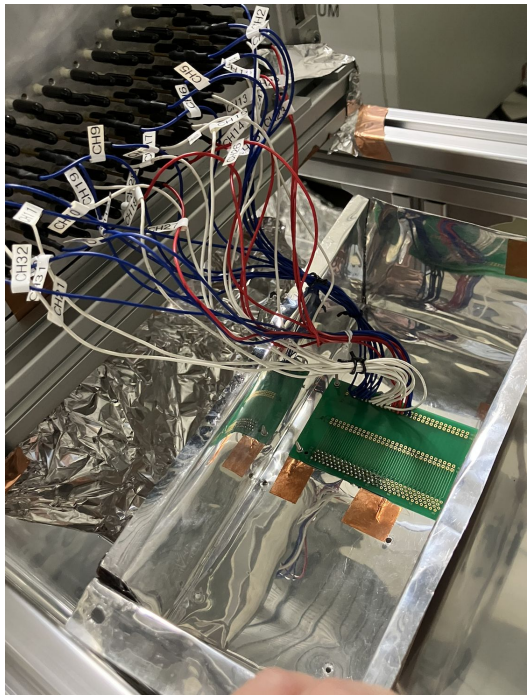


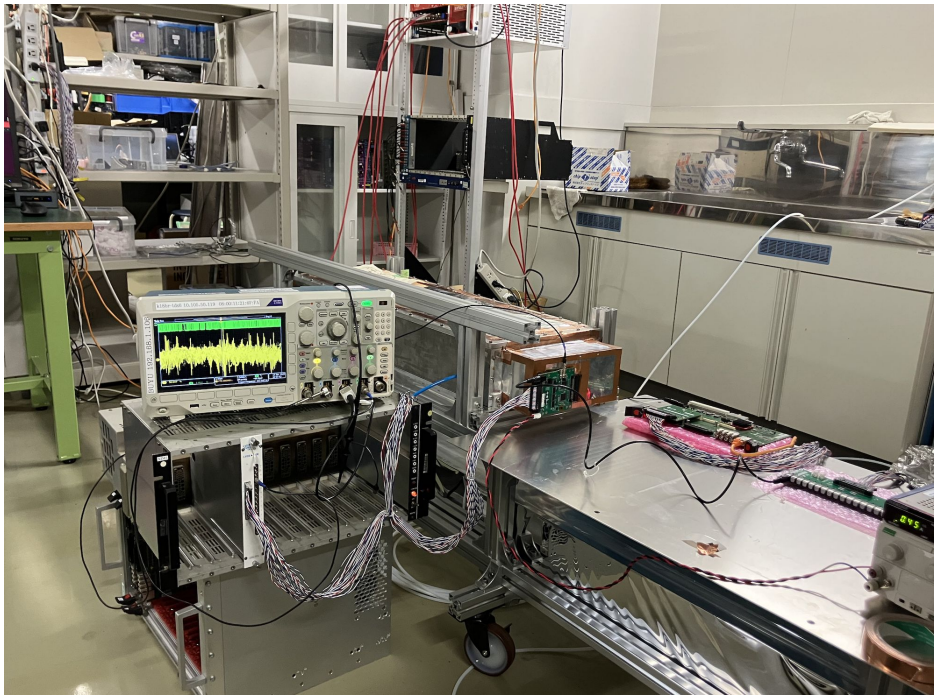
5: ASAGI x E15-TC

Sorry for no signal photo…

But we successfully observed the signals of cosmic-rays and X-rays from 55Fe.

Noiseis should be reduced more and more to study the detection efficiency and so on.





Back up

ASAGI with 白鳥IN
@RIKEN
2025.06.13 ~ 14

Yuto Kimura

ASAGI v1.5
Vivado 2024.2.1
小王辺り.
① open hardware manager
auto conect
mt 2569 L128 v118
close target
② HUL 電源切る
また入れる

③ SITPC utility

任意のIp adress
に変えられる。

EEP ROMにアクセスする。

↳ デフォルトじゃない
設定値を読み込む

④ pingで確認

↳ 書き込み終わり

HULパッケージ？
(20230520)

git repository？

Colibとかいう謎ディレクトリ
make

Asagi - Controller - Main

→ src

ライブラリにデキトーにリンク張って

⑤ function Generator
→ オシロで確認
→ ASAGI test In
→ out
→ オシロ

⑥ function Generator
→ Injector
→ out → オシロ
Saturation が見えた。
パラメタファイルを書き換えて
応答を見た。

— 昼ごはん —

⑦ 午前中の復習

Discuss
・光コネクタを小さくできないか！
・フラットケーブルと
光ケーブルどっちを
長くするか。

※SPDI用光通信ケーブル
・5VのACアダプタ
2A、1Aとかで
十分だろう。
(HULとSCTボードの電源用)

- IP adress
- 熱をちゃんと逃がす構造　急務
- テストパルスのoffsetはゼロにすべし。
- ノイズレベルは?
  → いい状態で2mVくらい

→パラメータの説明

⑧ ＋も－もなんでもOK.
通常－にInput
＋はGND.

※ CSAとPZCの比を2にするとテールをおさえられる。

飽和はDynamic Rangeに依存する。
(||| $V_{th} = -6.5\,mV$)

⑨ 自分で param file
書き換え. SCPで
転送. → 動かした。

Input 電荷
1 pC ~ 3 pC

ここら辺で線形性確認
すべし（宿題）

Injectorの容量は1pF

→
$Q = CV = 1\,pF \times 1\,V$
$= 1\,pC$

⑩ LVDS → NIM
で Discri 後の
Degital Signal
というメータにじっと
何かパターンが見えみた。

⑪ Injectorは3Vまで
（3pC）

(12) 注意点.

- TDCとるときは
  Leading tracing
  が奇数chと偶数ch
  で逆になる。
  (Do polを交互にしたい。)
  ↑これは、まわりこみ発振
  をおさえるため。

What to do?

- 入力の電荷を見つもって
  テストチャンバーのGainが
  わかる。
- Pulse Generatorで
  任意の波形作る?
- 電荷は同じで波形が
  違う場合は
  ASAGIでどう違いが
  見えるか

当最適なパラメータを
決める。

↑
まずこれが先か。